

KASUKABE *et al.*, SN 10/676,609  
Amdt. dated 03/22/2005  
Reply to OA mailed 09/22/2004

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**IN THE CLAIMS:**

1. (Currently Amended) A probe sheet comprising:

~~contact terminals that get into~~ arranged in a first surface of the probe sheet to  
oppose a wafer part to contact with electrodes provided on ~~a the~~ wafer;

wirings, each being drawn from one of said contact terminals in the probe  
sheet; and

electrode pads, each being arranged in second surface of the probe sheet at  
an opposite side thereof to the first surface and electrically connected to one of said  
wirings,

wherein a pitch ~~of between~~ said electrode pads in the second surface of the  
probe sheet is wider than a pitch ~~of between~~ said contact terminals in the first  
surface thereof.

2. (Currently Amended) The probe sheet according to claim 1,  
wherein said contact terminals are arranged according to an array of  
peripheral electrodes of semiconductor devices formed on said wafer part, and  
wherein said electrode pads are arranged in a grid pattern.

3. (Currently Amended) The probe sheet according to claim 1,  
wherein a metallic sheet, from which at least a part corresponding to signal  
electrode pads of the electrode pads is removed, is provided on the second surface  
of the probe sheet.

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4. (Currently Amended) The probe sheet according to claim 3,  
wherein a linear expansion coefficient of said metallic sheet is ~~almost equal to~~  
a linear expansion coefficient of said wafer part.

5. (Currently Amended) The probe sheet according to claim 3,  
wherein said metallic sheet is a 42 alloy sheet.

6. (Currently Amended) The probe sheet according to claim 1,  
wherein dummy terminals, each of which has a larger contact area with the  
wafer part than that of each of said contact terminal, ~~are terminals, are~~ provided on a  
the first surface of the probe sheet on which said contact terminals are provided.

7. (Currently Amended) The probe sheet according to claim 1,  
wherein said contact terminals are ~~created each~~ each created by using an  
anisotropically etched hole in a crystalline substrate as a cast.

8. (Currently Amended) A probe card comprising:  
a probe sheet having contact terminals ~~that get into~~ being arranged in a first  
surface of the probe sheet to oppose a wafer part to contact with electrodes provided  
on ~~a the wafer part~~, wirings each being drawn from one of the contact terminals, and  
electrode pads each being arranged in a second surface of the probe sheet at an  
opposite side thereof to the first surface and electrically connected to one of said  
wirings; and

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a multi-layer wiring substrate ~~on which electrodes, which are being provided~~  
at an opposite side of the probe sheet to the wafer part to face the second surface  
thereof, the multi-layer wiring substrate has electrodes each being electrically  
connected to one of said contact terminals, are provided terminals through the one of  
the electrode pads and formed on a surface opposed to the wafer of the multi-layer  
wiring substrate, and

wherein a pitch of ~~said electrodes provided on the surface of said multi-layer~~  
~~wiring substrate opposed to the wafer~~ between the electrode pads in the second  
surface of the probe sheet is wider than a pitch of between said contact terminals in  
the first surface thereof.

9. (Currently Amended) The probe card according to claim 8,

wherein said contact terminals of the probe sheet are arranged according to  
an array of peripheral electrodes of semiconductor devices formed on the surface of  
the wafer part, and

wherein the electrodes of said multi-layer wiring substrate are arranged in a  
grid pattern in the surface thereof.

10. (Currently Amended) The probe card according to claim 8,

wherein the electrodes of said multi-layer wiring substrate are provided in a  
device-opposed-area on the surface of said multi-layer wiring substrate.

11. (Currently Amended) The probe card according to claim 8,

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wherein at least one of capacitors, ~~resistors~~, or resistors or fuses are mounted in ~~the~~ a device-opposed area on said multi-layer wiring substrate.

12. (Currently Amended) The probe card according to claim 8,  
wherein the ~~electrodes of said contact terminals~~ electrode pads arranged in the second surface of the probe sheet and the electrodes of said multi-layer wiring substrate are electrically connected by a connection part ~~provided almost~~ extended vertically with respect said multi-layer wiring substrate.

13. (Currently Amended) The probe card according to claim 8,  
wherein ~~a connection between the electrodes of said contact terminals and the electrodes of said multi-layer wiring substrate is made via wires drawn from the contact terminals, are electrically connected to the electrode pads connected to said wires and having a pitch wider than a pitch of said contact terminals, and arranged in the second surface of the probe sheet via spring probes electrically connected to said electrode pads disposed therebetween.~~

14. (Currently Amended) The probe card according to claim 13,  
wherein said spring probes are removable.

15. (Currently Amended) The probe card according to claim 8,  
wherein ~~a connection between the electrodes of said contact terminals and each of the electrodes of said multi-layer wiring substrate is made via wirings drawn~~

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~~from said contact terminals, and each of the~~ electrode pads connected to said  
~~wirings and having a pitch wider than a pitch of said contact terminals, and arranged~~  
~~in the second surface of the problem sheet are~~ electrically connected to said  
~~electrode pads each other via a wire extended therebetween.~~

16. (Currently Amended) The probe card according to claim 8,  
wherein said probe card has a temperature adjustment function.

17. (Currently Amended) The probe card according to claim 8,  
wherein said contact terminals are each a pyramid-shaped or truncated-  
pyramid-shaped terminal created by using an anisotropically etched hole in a  
crystalline substrate as a cast.

18. (Currently Amended) Semiconductor test equipment comprising:  
a stage on which a wafer part is mounted; and  
a probe card having contact terminals that get in contact with electrodes of  
semiconductor devices formed on the wafer part and electrically connected to a  
tester that tests electrical characteristics of the semiconductor devices,  
wherein said probe card comprises:

a probe sheet having the contact terminals being arranged in a first  
surface of the probe sheet opposite to the wafer part, wirings each being  
drawn from one of the contact terminals, and electrode pads each being

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arranged in a second surface of the probe sheet at an opposite side thereof to the first surface and electrically connection to one of said wirings; and  
a multi-layer wiring substrate whose electrodes electrically connected to the contact terminals via the electrode pads respectively are provided on a surface opposed to the wafer part across the probe sheet, and  
wherein a pitch ~~of the electrodes of said multi-layer wiring substrate provided on the surface opposed to the wafer~~ between the electrode pads in the second surface of the probe sheet is wider than a pitch ~~of~~ between said contact terminals.

19. (Currently Amended) Semiconductor test equipment according to claim 18,  
wherein a temperature of the stage and the probe card can both be controlled.

20. (Currently Amended) The semiconductor test equipment according to claim 18,  
wherein said contact terminals are each a pyramid-shaped or truncated-pyramid-shaped terminal created with an anisotropically etched hole in a crystalline substrate as a shape former.

21. (New) The probe card according to claim 10,  
wherein the device-opposed area is an area of the multi-layer wiring substrate opposite to semiconductor devices formed on the surface of the wafer part across the probe sheet.

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22. (New) The probe card according to claim 11,

wherein the device-opposed area is an area of the multi-layer wiring substrate opposite to semiconductor devices formed on the surface of the wafer part across the probe sheet, and that at least one of capacitors, resistors or fuses are mounted on a surface of the multi-layer wiring substrate at an opposite side thereof to the wafer part.

23. (New) A probe sheet comprising:

contact terminals arranged in a first surface of the probe sheet to oppose a wafer part to contact with electrodes provided on the wafer part;

wirings, each being drawn from one of said contact terminals in the probe sheet; and

electrode pads, each being arranged in a second surface of the probe sheet at an opposite side thereof to the first surface and electrically connected to one of said wirings,

wherein a pitch between said electrode pads in the second surface of the probe sheet is wider than a pitch between said contact terminals in the first surface thereof, and wherein ones of said electrode pads extending in a direction away from an area of the contact terminals are laid out in an array having at least three rows extending at least somewhat parallel to the area.

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24. (New) A probe sheet as claimed in claim 23, wherein the electrode pads of a subject row of the rows, are staggered with respect to the electrode pads of a neighboring row.

25. (New) A probe sheet as claimed in claim 23, wherein the wirings are serpentine wirings, and ones of the serpentine wirings trace serpentine paths between the electrode pads.

26. (New) A probe sheet as claimed in claim 25, wherein a pitch between ones of the serpentine wirings varies extending in the direction away from the area of the contact terminals.